Ei Wave Digitech (I) Pvt

PICO-FILTER (30 MHz - 1000MHz)

EI WAVE DIGITECH (I) PVT LTD

EIWAVE DIGITECH (I) PVT LTD.,

#8-2-693/2/29, Mithila Nagar,
Road No.12, Banjara Hills,
Hyderabad - 500034

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Tunable Filter (30 -1000 MHz)

Description:

PICO FILTER are designed for low power application. The ultra-miniature size of the filter makes it unique with this specification. It comes with an overall dimension of 20 x 20 x 5.5 (mm). Module is designed with surface mount package with metallic shield. Filters are available over the frequency range of 30MHz-1000MHz.

Specifications:Pin Description and Ratings:

Frequency Coverage:	30- 1000 MHz
Input/output Impedance	50 Ω
In-band Input/output VSWR	2:1 min
In-band RF Power Handling	+6dBm
In-band third Order Intercept Point	+16dBm
Tuning Control	Serial
Tuning Speed	20µs typical
Operating Temperature Range	-40 ºC to +85 ºC
Size	20 x 20 x 5.5 (mm) (LxBxH)
Package	SMD

Pin	Reference	Description	Maximum rating
1	GND	Ground	--
2	SCLK	Serial clock	+3.3V
3	SDI	Serial Data	+3.3V
4	CS	Chip select	+3.3V
5,6,7	NC	No connection	--
8	VCC	+5V supply	+5.5V
9	GND	Ground	--
10	VDD	+28V supply	+28V
11-27	GND	Ground	--

General Information

The filter module requires two supply voltages: **+5V** DC digital supply and **+28V**DC analog supply. These supply voltages should be adequately filtered as noise present on these pins will influence the RF signal purity. Frequency control signals are 3.3V logic level only.

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Digital Interface Information:

The digital interface format is SPI.

Filter selection

Frequency Range	Suffix	Insertion Loss	% Bandwidth (3dB)	Shape Factor (30 dB / 3 dB)
30 to 90 MHz	-10	7	10	7
90 to 220MHz	-5	7.5	5	7
	-8	4.5	8	7
	-10	3.5	10	7
220 to 512 MHz	-3	8.5	3	7.5
	-5	5.5	5	6.5
	-8	4	8	6
	-10	3	10	6
500 to 1000 MHz	-5	6.5	5	7
	-8	5.5	8	6
	-10	4	10	6

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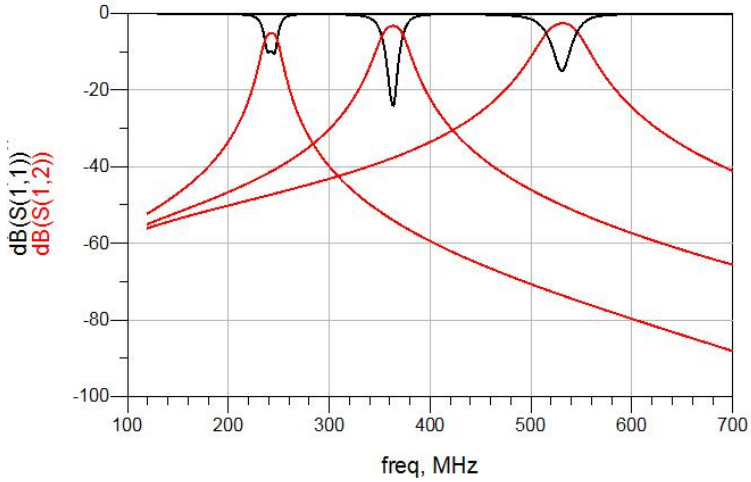
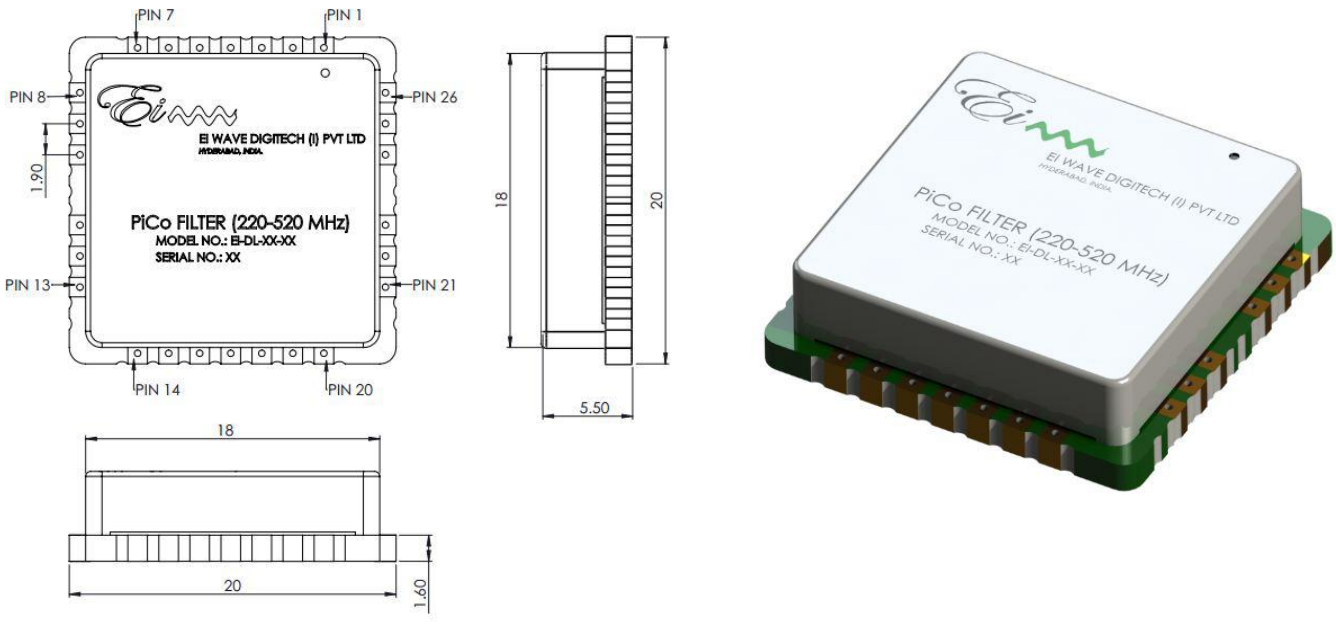
Performance:

The following plots illustrate approximate performance:



Mechanical Outline:



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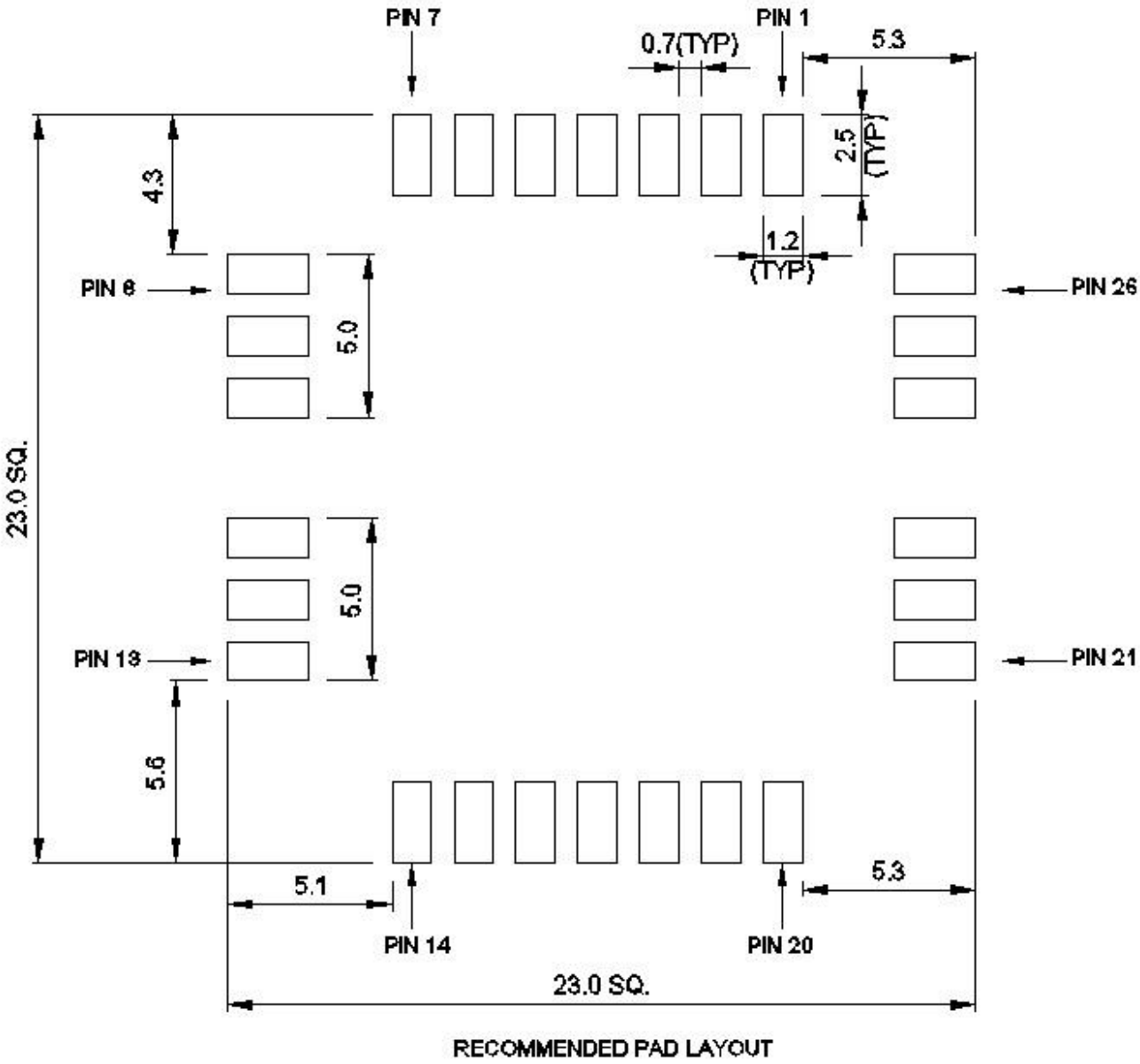
Recommended Pad Layout:



RECOMMENDED PAD LAYOUT

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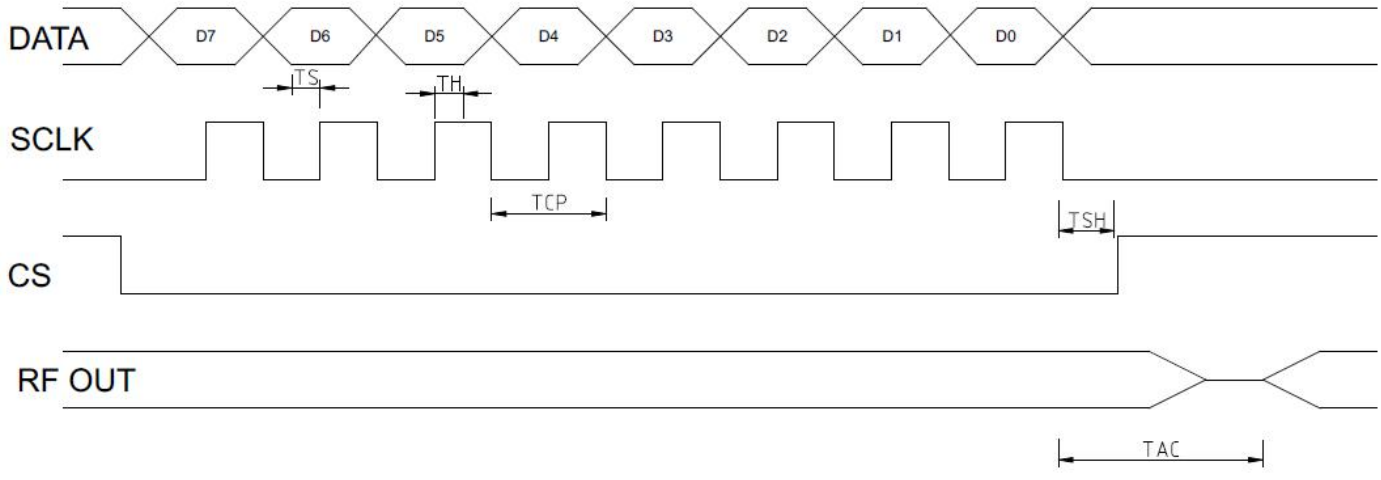
SPI Signal description and Timing diagram

The SPI has a 3-wire synchronous serial interface. Data communication is enabled with a Chip Select wire (CS). Data is transmitted with a 3-wire interface consisting of wires for serial data input (SDI), chip select input (CS) and serial clock (SCK).The description is given in table below:

Name	Type	Description
SCLK	Input	SPI Clock input (5MHz max)
SDI	Input	SPI Serial data input
CS	Input	SPI Chip Select input

Each transmission starts with a rising edge of CS and ends with the falling edge. During transmission, commands and data are controlled by SPICLK and CS according to the following rules:

SPI Data Read Cycle:



Time	Description	Min	Max	Unit
T_S	Serial Data setup Time	100	-	ns
T_H	Serial Data Hold Time	100	-	ns
T_{CP}	Clock Period	200	-	ns
T_{SH}	Chip Select Pulse Width	100		ns
T_{AC}	Access time from CS to Fo		100	us
T_{NEW}	Delay between new frequency command	500		us

Description:

- Data received width is 8 Bit in one SPI chip select input.
- Time required between one SPI chip select to another SPI chip select is 500us.
- It receives MSB data first and LSB last.
- Data is sampled on rising edge of SPI clock and shifted at falling edge of SPI clock.
- Maximum SPI clock frequency is 5MHz.
- The SPI interface is standard mode 0 (CPOL = 0, CPHA = 0)